PAT-NO: JP02001127039A

DOCUMENT-IDENTIFIER: JP 2001127039 A

TITLE: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

PUBN-DATE: May 11, 2001

INVENTOR-INFORMATION:

| NAME | COUNTRY |
|---|---|
| SATO, MASAYUKI | N/A |

ASSIGNEE-INFORMATION:

| NAME | COUNTRY |
|---|---|
| NEC CORP | N/A |


APPL-NO: JP11302329

APPL-DATE: October 25, 1999

INT-CL (IPC): H01L021/3065, H01L021/316

ABSTRACT:

PROBLEM TO BE SOLVED: To dissolve the problems in conventional manufacturing method such as not only the flaking of a silicon film but also the drop in selectivity with resist, the peeling of the deposition at one sidewall of an etching chamber, etc., for the selectivity between the silicon film and the nitride film drops when the flow rate of oxygen is increased to raise the drillability in etching of a nitride film, using CHF3/O2/Ar mixed gas for removal of the nitride film for opening of a contact, in the element structure which has a nitride film on the silicon film including a silicon substrate.

SOLUTION: When C4F8/CH2F2/Ar/O2 mixed gas is used for etching of a nitride film 4, the etching of the nitride film 4 is accelerated, and also since CHxFY gas is one which is high in deposition effect, the selectivity to a silicon substrate 1 rises, and further the etching can be made continuously in roughly the same etching gas as that for the interlayer oxide film covering the nitride film 4, so stable etching excellent in productivity becomes possible.

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号
特開2001－127039
（P2001－127039A）
(43)公開日　平成13年5月11日(2001.5.11)

| (51)Int.Cl.⁷ | 識別記号 | F I | テーマコード*(参考) |
|---|---|---|---|
| H01L 21/3065 | | H01L 21/316 | M 5F004 |
| 21/316 | | 21/302 | F 5F058 |

審査請求　有　　請求項の数8　OL　（全 5 頁）

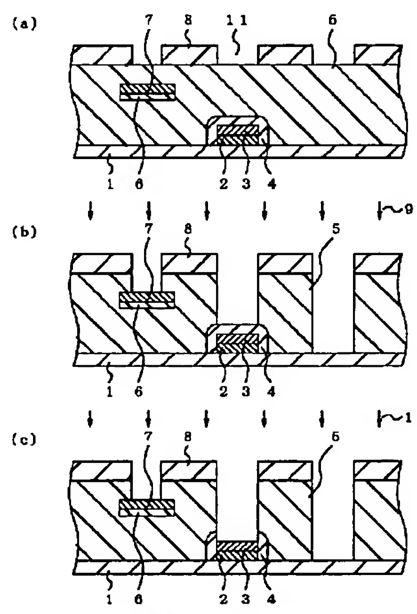
(21)出願番号　特願平11－302329
(22)出願日　平成11年10月25日(1999.10.25)

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目7番1号
(72)発明者　佐藤　聖幸
東京都港区芝五丁目7番1号　日本電気株式会社内
(74)代理人　100082935
弁理士　京本　直樹　（外2名）

Fターム(参考)　5F004 BA04 BB11 DA00 DA15 DA16 DA23 DA26 DA30 DB00 DB03 EA28 EB01
5F058 BC02 BC07 BD01 BH12

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】シリコン基板を含むシリコン膜の上に窒化膜を有する素子構造では、コンタクト開口のための窒化膜除去にＣＨＦ３／$O_2$／Ａｒ混合ガス等を用い、窒化膜エッチングにおける抜け性を上げるため酸素流量を増加させるとシリコン膜と窒化膜との選択性が低下し、シリコン膜の削れのみならず、レジストとの選択性の低下、エッチングチャンバー側壁のデポの剥がれ等が問題となっていた。
【解決手段】窒化膜４のエッチングに$C_4F_8$／$CH_2F_2$／Ａｒ／$O_2$混合ガスを用いると、窒化膜４のエッチングが促進されると共に、ＣＨｘＦｙガスはデポジション効果が高いガスであるため、シリコン基板１に対しての選択性が向上し、更に、窒化膜４の上を覆う層間酸化膜５のエッチングガス系とほぼ同等のエッチングガス系で連続してエッチングできるため、安定した、生産性の良いエッチングが可能となる。




1：シリコン基板　6：酸化タンタル
2：ポリシリコンゲート　7：容量ポリシリプレート
3：WSi　8：フォトレジスト
4：窒化膜　9，10：混合ガス
5：層間酸化膜　11：コンタクト

【特許請求の範囲】

【請求項１】　基板の上方に、下層が窒化膜、上層が酸化膜からなる積層膜を形成し、第１エッチングガスを用いて前記酸化膜を選択的にエッチング除去して前記酸化膜に開口部を形成し、第２エッチングガスを用いて前記開口部を通して前記窒化膜をエッチング除去する半導体装置の製造方法であって、前記第２エッチングガスは、ＣｘＦｙを主反応ガスとした混合ガスからなることを特徴とする半導体装置の製造方法。

【請求項２】　前記第２エッチングガスのＣｘＦｙは、$C_3F_6$、$C_4F_6$、$C_4F_8$、$C_5F_8$のうちのいずれかのガスである請求項１記載の半導体装置の製造方法。

【請求項３】　前記第２エッチングガスは、$CH_2F_2$、$CH_3F$、$CH_3Br$、$NH_3$、$C_2H_5OH$、$CH_3OH$のうちのいずれかのガスを添加ガスとして含む請求項２記載の半導体装置の製造方法。

【請求項４】　前記第２エッチングガスは、ＣＯ、$CO_2$のうちのいずれかのガスを添加ガスとして含む請求項２記載の半導体装置の製造方法。

【請求項５】　前記第１エッチングガスは、前記第２エッチングガスの主反応ガスと同じＣｘＦｙを主反応ガスとする混合ガスである請求項２、３又は４記載の半導体装置の製造方法。

【請求項６】　前記第１エッチングガスは、添加ガスとしてＣＯ、$CO_2$のうちのいずれかのガスを含む請求項５記載の半導体装置の製造方法。

【請求項７】　前記第１エッチングガス及び前記第２エッチングガスは共にＡｒ及び$O_2$を含む請求項１、２、３、４、５又は６記載の半導体装置の製造方法。

【請求項８】　前記第２エッチングガスによるエッチング工程は、前記第１エッチングガスによるエッチング工程に続いて前記第１エッチングと同一チャンバー内で連続して行われる請求項１、２、３、４、５、６又は7記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置の製造方法に関し、特にシリコン膜の上に窒化膜、酸化膜が形成された構成の素子に対して接続を取るためのコンタクトの形成方法に関する。

【０００２】

【従来の技術】近年、半導体装置の分野では益々進行し、例えば超ＬＳＩについてその微細化が進み、コンタクト形成工程におけるフォトリソグラフィー技術の目合わせマージンの確保が困難になってきている。そこで、コンタクト形成工程においてゲート電極を窒化膜で覆い窒化膜をストッパー膜としたコンタクトエッチング技術のセルフアラインコンタクト（ＳＡＣ）技術が広く用いられるようなってきた。

【０００３】

【発明が解決しようとする課題】しかしながら、セルフアラインコンタクトプロセスでは、ゲート電極を絶縁膜である窒化膜で覆い、その上に酸化膜等の層間絶縁膜が覆っているため、ゲート電極との接続を取るために、コンタクトエッチングにより層間絶縁膜にコンタクトを形成し、更に窒化膜を除去する必要がある。このコンタクトエッチング後の窒化膜除去には、従来ＣＨＦ３／$O_2$／Ａｒ混合ガス等が用いられてきたが、コンタクトのアスペクト比が高くなるに従い、窒化膜エッチングステップにおける抜け性を上げるため酸素流量を増加させる必要があった。そのため、窒化膜エッチング時に露出している容量ポリシリプレートやシリコン基板と窒化膜との選択性が低下し、容量ポリシリの突き抜けやシリコン基板の削れのみならず、レジストとの選択性の低下によるコンタクト径の広がり、エッチングチャンバー側壁に堆積したデポジションの剥がれによるゴミの多発、コンタクトエッチングステップと窒化膜エッチングステップのエッチングガス系の違いによるチャンバー雰囲気の変化によるプロセスの不安定性が問題であった。

【０００４】本発明の目的は、窒化膜と酸化膜の積層構造からなる層間膜のドライエッチングにおいて、レジスト及びシリコンとの選択比の向上をすることができ、且つ、ゴミの発生を抑制しチャンバー雰囲気を変えることなく高い生産性が可能となる半導体装置の製造方法を提供することにある。

【０００５】

【課題を解決するための手段】本発明の半導体装置の製造方法は、基板の上方に、下層が窒化膜、上層が酸化膜からなる積層膜を形成し、第１エッチングガスを用いて前記酸化膜を選択的にエッチング除去して前記酸化膜に開口部を形成し、第２エッチングガスを用いて前記開口部を通して前記窒化膜をエッチング除去する半導体装置の製造方法であって、前記第２エッチングガスは、ＣｘＦｙを主反応ガスとした混合ガスからなることを特徴とし、前記第２エッチングガスのＣｘＦｙは、$C_3F_6$、$C_4F_6$、$C_4F_8$、$C_5F_8$のうちのいずれかのガスであり、前記第２エッチングガスは、$CH_2F_2$、$CH_3F$、$CH_3Br$、$NH_3$、$C_2H_5OH$、$CH_3OH$のうちのいずれかのガスを添加ガスとして含む、或いは、前記第２エッチングガスは、ＣＯ、$CO_2$のうちのいずれかのガスを添加ガスとして含む、というものである。

【０００６】又、上記半導体装置の製造方法において、前記第１エッチングガスは、前記第２エッチングガスの主反応ガスと同じＣｘＦｙを主反応ガスとする混合ガスであり、前記第１エッチングガスは、添加ガスとしてＣＯ、$CO_2$のうちのいずれかのガスを含み、前記第１エッチングガス及び前記第２エッチングガスは共にＡｒ及び$O_2$を含む、というものである。

【０００７】最後に、上記半導体装置の製造方法において、前記第２エッチングガスによるエッチング工程は、

前記第１エッチングガスによるエッチング工程に続いて前記第１エッチングと同一チャンバー内で連続して行われる、というものである。

【０００８】

【発明の実施の形態】まず、本発明の第１の実施形態について、図１（ａ）～（ｃ）を用いて説明する。本実施形態は、酸化タンタル膜等を容量とするＤＲＡＭで、コンタクトのアスペクト比が大きい場合のコンタクトエッチングを例として示したもので、図1は、コンタクトエッチングチップ前後の半導体装置の製造方法を工程順に示す断面図である。

【０００９】図１（ａ）に示すように、シリコン基板１上にゲート電極を構成するポリシリコンゲート２、タングステンシリサイド（ＷＳｉ）３及びそれを覆う窒化膜４、さらにシリコン基板１及び窒化膜４を覆う層間酸化膜５、層間酸化膜５中に設けられる容量を構成する酸化タンタル（Ｔａ２Ｏ５）６、容量ポリシリプレート７とが形成され、フォトリソグラフィー技法によって、コンタクト１１を有するパターンをフォトレジストに転写して、フォトレジスト８を形成する。

【００１０】次に、図１（ｂ）に示すように、2周波ＲＩＥ（Ｒｅａｃｔｉｖｅ　ＩｏｎＥｔｃｈｉｎｇ）ドライエッチング装置を用いて、フォトレジスト８をマスクとして、層間酸化膜５の一番厚い膜厚分までのエッチング（ジャストエッチング）を$C_4F_8$／ＣＯ／Ａｒ／$O_2$混合ガス９でドライエッチングする。この時の条件は、圧力５．３３Ｐａの下に、$C_4F_8$を２０ｓｃｃｍ、ＣＯを４０ｓｃｃｍ、Ａｒを５００ｓｃｃｍ、$O_2$を９ｓｃｃｍ流し、上部電極に２７ＭＨｚ、２２００Ｗの高周波電力を印加し、基板には８００ｋＨｚ、１４００Ｗの高周波電力を印加し、上部電極と下部電極との間隔を２０ｍｍに設定し、基板温度を－２０℃とした。その結果、層間酸化膜５のエッチングレートは７３０ｎｍ／ｍｉｎ、フォトレジストのエッチングレートは７９ｎｍ／ｍｉｎ、層間酸化膜５とフォトレジスト８のエッチング速度比（選択比）は、約9倍となっている。

【００１１】上記層間酸化膜のエッチングにおいては、高アスペクト比のコンタクトへエッチングガスを浸透させるために、混合ガスにＣＯを添加することが有効である。

【００１２】引き続き、図１（ｃ）に示すように、窒化膜４を$C_4F_8$／$CH_2F_2$／Ａｒ／$O_2$混合ガス１０でドライエッチングする。この時の条件は、圧力５．３３Ｐａの下に、$C_4F_8$を１０ｓｃｃｍ、$CH_2F_2$を２０ｓｃｃｍ、Ａｒを５００ｓｃｃｍ、$O_2$を１５ｓｃｃｍ流し、上部電極に２７ＭＨｚ、２２００Ｗの高周波電力を印加し、基板には８００ｋＨｚ、１４００Ｗの高周波電力を印加し、上部電極と下部電極との間隔を２０ｍｍに設定し、基板温度を－２０℃とした。その結果、窒化膜４のエッチングレートは６１０ｎｍ／ｍｉｎ、層間酸化膜５のエッチングレートは５７０ｎｍ／ｍｉｎ、フォトレジストのエッチングレート３４ｎｍ／ｍｉｎ、シリコン基板１及び容量ポリシリプレート７のエッチレートは３ｎｍ／ｍｉｎ、窒化膜４と層間酸化膜５のエッチング速度比（選択比）は約　１．１倍、窒化膜４とシリコン基板１及び容量ポリシリプレート７のエッチング速度比（選択比）は約２００倍、層間酸化膜５とシリコン基板１及び容量ポリシリプレート７のエッチング速度比（選択比）は約１９０倍となった。また、そのエッチング形状は異方的なものとなった。

【００１３】ここで、窒化膜の層間酸化膜に対するエッチング速度比（選択比）は約　１．１倍と低いが、窒化膜エッチングは、窒化膜除去だけでなく、上記層間酸化膜のエッチング工程における層間酸化膜のジャストエッチングに対する追加エッチング（オーバーエッチング）の役割をも果たしている。

【００１４】本発明の第１の実施形態によれば、窒化膜のエッチングステップにおいて、フロロカーボンガスにＣＨｘＦｙガス等の水素原子を含むガスを添加することで、ＣＨｘＦｙのＣ及びＨが窒化膜のＮと結合しＣ－Ｎ及びＮ－Ｈが生成されることにより、窒化膜のエッチングが促進される。

【００１５】また、ＣＨｘＦｙガスはデポジション効果が高いガスであるため、シリコンに対しての選択性が向上すると共に、窒化膜エッチングステップにコンタクトエッチングステップにおいて使用する層間酸化膜のエッチングガス系とほぼ同等のエッチングガス系を用いているため、エッチングチャンバーの雰囲気を変えることなく安定したエッチングが可能となる。

【００１６】次に、本発明の第２の実施形態について、図２（ａ）～（ｃ）を用いて説明する。本実施形態は、コンタクトのアスペクト比がさほど大きくないＳＲＡＭの場合のコンタクトエッチングを例として示したもので、図2は、コンタクトエッチングチップ前後の半導体装置の製造方法を工程順に示す断面図である。

【００１７】図２（ａ）に示すように、シリコン基板３１上にゲート電極を構成するポリシリコンゲート３２、タングステンシリサイド（ＷＳｉ）３３とそれらの側面を保護するサイドウォール３６と、シリコン基板３１及びゲート電極を覆う窒化膜３４と、窒化膜３４を覆う層間酸化膜３５が形成され、フォトリソグラフィー技法によって、コンタクト４１を有するパターンをフォトレジストに転写して、フォトレジスト３８を形成する。

【００１８】次に、図２（ｂ）に示すように、2周波ＲＩＥ（Ｒｅａｃｔｉｖｅ　ＩｏｎＥｔｃｈｉｎｇ）ドライエッチング装置を用いて、フォトレジスト３８をマスクとして、層間酸化膜３５の膜厚分までのエッチング（ジャストエッチング）を$C_4F_8$／Ａｒ／$O_2$混合ガスプラズマ３９でドライエッチングする。この時の条件は、圧力６．６７Ｐａの下に、$C_4F_8$を７ｓｃｃｍ、Ａ

ｒを６００ｓｃｃｍ、$O_2$を２ｓｃｃｍ流し、上部電極に２７ＭＨｚ、２０００Ｗの高周波電力を印加し、基板には８００ｋＨｚ、８００Ｗの高周波電力を印加し、上部電極と下部電極との間隔を２４ｍｍに設定し、基板温度を＋２０℃とした。その結果、層間酸化膜３５のエッチングレートは４２０ｎｍ／ｍｉｎ、フォトレジストのエッチングレートは２８ｎｍ／ｍｉｎ、層間酸化膜３５とフォトレジスト３８のエッチング速度比（選択比）は、約１５倍、層間酸化膜３５と窒化膜３４のエッチング速度比（選択比）は約２０倍となった。

【００１９】ここで、層間酸化膜のエッチングにおいては、コンタクトのアスペクト比が第１の実施形態ほど高くなく、混合ガスにＣＯを添加する必要はない。

【００２０】引き続き、図２（ｃ）に示すように、窒化膜３４を$C_4F_8$／$CH_2F_2$／Ａｒ／$O_2$混合ガス４０でドライエッチングする。この時の条件は、圧力５．３３Ｐａの下に、$C_4F_8$を１０ｓｃｃｍ、$CH_2F_2$を２０ｓｃｃｍ、Ａｒを５００ｓｃｃｍ、$O_2$を１５ｓｃｃｍ流し、上部電極に２７ＭＨｚ、２２００Ｗの高周波電力を印加し、基板には８００ｋＨｚ、１４００Ｗの高周波電力を印加し、上部電極と下部電極との間隔を２０ｍｍに設定し、基板温度を＋２０℃とした。その結果、窒化膜３４のエッチングレートは６１０ｎｍ／ｍｉｎ、層間酸化膜３５のエッチングレートは５７０ｎｍ／ｍｉｎ、フォトレジストのエッチングレート３４ｎｍ／ｍｉｎ、シリコン基板３１のエッチレートは３ｎｍ／ｍｉｎ、窒化膜３４と層間酸化膜３５のエッチング速度比（選択比）は約　１．１倍、窒化膜３４とシリコン基板３１のエッチング速度比（選択比）は約２００倍、層間酸化膜３５とシリコン基板３１のエッチング速度比（選択比）は約１９０倍となった。また、そのエッチング形状は異方的なものとなった。

【００２１】本実施形態においても、第１の実施形態と同様に、窒化膜のエッチングステップにおける窒化膜エッチングの促進、シリコンに対してのエッチング選択性の向上、生産性の良いエッチング、が可能となる。

【００２２】尚、本発明の第１、２の実施形態においては窒化膜エッチングの主反応ガスに、$C_4F_8$ガスを用いたが、$C_3F_6$、$C_4F_6$、$C_5F_8$ガス等のフロロカーボンガスから成る群れから選択された少なくとも一種類を反応ガスに用いても同様の効果が得られる。

【００２３】また、本発明の第１、２の実施形態においては窒化膜エッチングの添加ガスに、$CH_2F_2$ガスを用いたがモノフルオロメタン（$CH_3F$）、臭化メチル（$CH_3Br$）、$C_xH_yOH$（$C_2H_5OH$、$CH_3OH$）等の水素原子を含むガスからなる群れから選択された少なくとも一種類を添加ガスに用いるか、或いは、一酸化炭素（ＣＯ）や二酸化炭素（$CO_2$）を添加ガスに用いても同様の効果が得られる。

【００２４】さらに、本発明の第１、２の実施形態においては層間酸化膜エッチングの主反応ガスに$C_4F_8$を用いたが、窒化膜エッチングの主反応ガスに合わせて、$C_3F_6$、$C_4F_6$、$C_5F_8$ガス等のフロロカーボンガスから成る群れから選択された少なくとも一種類を反応ガスに用いても同様の効果が得られ、本発明の第１の実施形態においては添加ガスとしては、一酸化炭素（ＣＯ）以外に二酸化炭素（$CO_2$）を用いても同様の効果が得られる。

【００２５】最後に、本発明の第１、２の実施形態においては窒化膜のエッチングステップに上記各実施形態の構成は単なる例示であり、本発明の半導体装置の製造方法は、上記構成からなる様々な修正及び変更を加えた半導体装置の製造方法を含むことは当然である。

【００２６】

【発明の効果】上述のように、窒化膜及び酸化膜の積層構造からなる層間絶縁膜のエッチングにおいて、酸化膜のエッチングに$C_4F_8$／ＣＯ／Ａｒ／$O_2$混合ガスを用い、引き続く窒化膜のエッチングに$C_4F_8$／$CH_2F_2$／Ａｒ／$O_2$混合ガスを用いることにより、窒化膜のエッチングが促進されると共に、$CH_xF_y$ガスはデポジション効果が高いガスであるため、シリコン膜に対しての選択性が向上し、更に、窒化膜エッチングステップにコンタクトエッチングステップにおいて使用する層間酸化膜のエッチングガス系とほぼ同等のエッチングガス系を用いているため、エッチングチャンバーの雰囲気を変えることなく安定した、生産性の良いエッチングが可能となる。

【図面の簡単な説明】

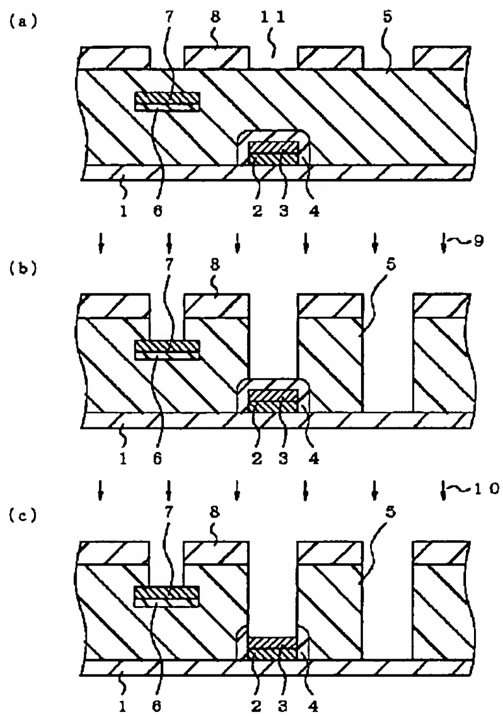
【図１】本発明の第１の実施形態の半導体装置の製造方法を工程順に示す断面図である。

【図２】本発明の第２の実施形態の半導体装置の製造方法を工程順に示す断面図である。

【符号の説明】

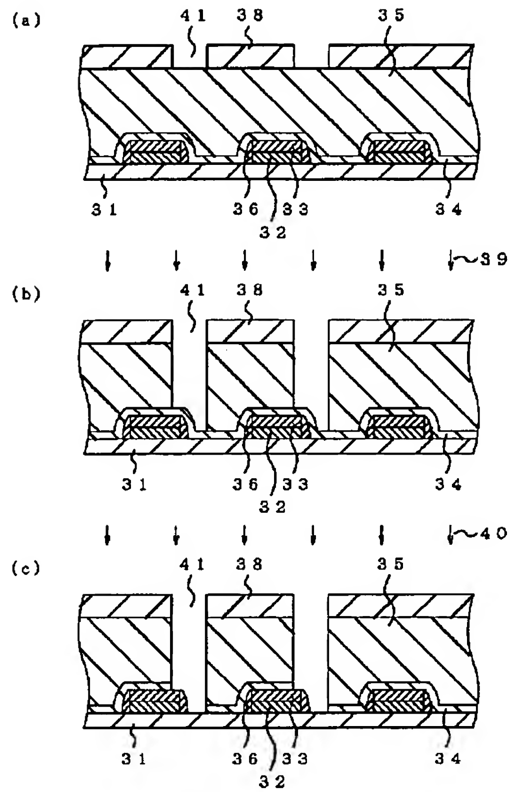
１、３１　シリコン半導体基板
２、３２　ポリシリコンゲート
３、３３　ＷＳｉ
４、３４　窒化膜
５、３５　層間酸化膜
６　酸化タンタル
７　容量ポリシリプレート
８、３８　フォトレジスト
９、１０、３９、４０　混合ガス
１１、４１　コンタクト
３６　サイドウォール

【図1】




1：シリコン基板
2：ポリシリコンゲート
3：WSi
4：窒化膜
5：層間酸化膜
6：酸化タンタル
7：容量ポリシリプレート
8：フォトレジスト
9，10：混合ガス
11：コンタクト

【図2】




31：シリコン基板
32：ポリシリコンゲート
33：WSi
34：窒化膜
35：層間酸化膜
36：サイドウォール
38：フォトレジスト
39，40：混合ガス
41：コンタクト

JP 2001-127039

* NOTICES *



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the formation approach of the contact for taking connection to the component of a configuration of that the nitride and the oxide film were formed on the silicone film about the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] In recent years, in the field of a semiconductor device, it goes on increasingly, for example, the detailed-ization progresses about a VLSI, and reservation of the eye doubling margin of the photolithography technique in a contact formation process is becoming difficult. Then, the self aryne contact (SAC) technique of the contact etching technique which used the bonnet nitride as the stopper film for the gate electrode by the nitride in the contact formation process has become as [ use / technique / widely ].
[0003]
[Problem(s) to be Solved by the Invention] However, since interlayer insulation films, such as an oxide film, have covered the gate electrode a bonnet and on it by the nitride which is an insulator layer, in order to take connection with a gate electrode, it is necessary to form contact in an interlayer insulation film by contact etching, and to remove a nitride further in a self aryne contact process. In order to raise the omission nature in a nitride etching step, the oxygen flow rate needed to be made to increase as the aspect ratio of contact becomes high although CHF3/O2-/Ar mixed gas etc. has been conventionally used for nitride clearance after this contact etching. Therefore, the instability of the process by change of the chamber ambient atmosphere by the difference between frequent occurrence of the dust by peeling of the deposition which the selectivity of the capacity polysilicon plate and the silicon substrate which have been exposed at the time of nitride etching, and a nitride fell, could delete the thrust omission of capacity polysilicon and the silicon substrate, and did not come to accept, but was deposited on the breadth of the diameter of contact by lowering of selectivity with a resist and an etching chamber side attachment wall, and the etching gas system of a contact etching step and a nitride etching step was a problem.
[0004] The object of this invention is in the dry etching of the interlayer film which

consists of a laminated structure of a nitride and an oxide film to offer the manufacture approach of the semiconductor device whose high productivity becomes possible, without being able to carry out improvement in a selection ratio with a resist and silicon, and controlling generating of dust, and changing a chamber ambient atmosphere.

[0005]

[Means for Solving the Problem] As for the manufacture approach of the semiconductor device of this invention, a lower layer forms [ a nitride and the upper layer ] the cascade screen which consists of an oxide film above a substrate. Carry out etching clearance of said oxide film selectively using the 1st etching gas, and opening is formed in said oxide film. It is the manufacture approach of the semiconductor device which carries out etching clearance of said nitride through said opening using the 2nd etching gas. Said 2nd etching gas It is characterized by consisting of mixed gas which made CxFy main reaction gas. CxFy of said 2nd etching gas It is gas of C3F6, C4F6, C4F8, or C5F8. Said 2nd etching gas CH2F2, CH3F, and CH3 -- the gas of the Br, NH3, C2H5OH, or the CH3OH(s) is included by said 2nd etching gas as addition gas, or the gas of either CO or COs2 is included as addition gas

[0006] Moreover, in the manufacture approach of the above-mentioned semiconductor device, said 1st etching gas is mixed gas which makes the same CxFy as the main reaction gas of said 2nd etching gas main reaction gas, and, in said 1st etching gas, said both 1st etching gas and said 2nd etching gas contain Ar and O2 including the gas of either CO or CO2 as addition gas.

[0007] In the manufacture approach of the above-mentioned semiconductor device, the etching process by said 2nd etching gas is continuously performed at the last within the same chamber as said 1st etching following the etching process by said 1st etching gas.

[0008]

[Embodiment of the Invention] First, the 1st operation gestalt of this invention is explained using drawing 1 (a) - (c). This operation gestalt is DRAM which makes the tantalum oxide film etc. capacity, it is what showed contact etching when the aspect ratio of contact is large as an example, and drawing 1 is the sectional view showing the manufacture approach of the semiconductor device before and behind a contact etching chip in order of a process.

[0009] As shown in drawing 1 (a), the wrap nitride 4, the tantalum oxide (Ta 2O5) 6 which constitutes the capacity in which a silicon substrate 1 and a nitride 4 are further formed into the wrap interlayer oxide film 5 and an interlayer oxide film 5, and the capacity polysilicon plate 7 are formed on a silicon substrate 1 in the polish recon gate 2, the tungsten silicide (WSi) 3, and it which constitute a gate electrode, by photolithography technique, the pattern which has contact 11 is imprinted to a photoresist, and a photoresist 8 is formed.

[0010] Next, as shown in drawing 1 (b), dry etching of the etching (just etching) to a part for the thickest thickness of an interlayer oxide film 5 is carried out with C4F8 / CO/Ar/O2 mixed gas 9 by using a photoresist 8 as a mask using a 2 cycle RIE (Reactive IonEtching) dry etching system. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 40sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ C4F8 / 20sccm(s) and CO ] to 9sccm sink and the up electrode for O2, the high-frequency power of 800kHz and 1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into -20 degrees C. Consequently, in the etching rate of

730 nm/min and a photoresist, the etching velocity ratio (selection ratio) of 79 nm/min, an interlayer oxide film 5, and a photoresist 8 is [ the etching rate of an interlayer oxide film 5 ] about 9 times.
[0011] In etching of the above-mentioned interlayer oxide film, in order to make etching gas permeate contact of a high aspect ratio, it is effective in mixed gas to add CO.
[0012] Then, as shown in drawing 1 (c), dry etching of the nitride 4 is carried out with C4F8/CH2F2/Ar/O2 mixed gas 10. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 20sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ C4F8 / 10sccm(s) and CH2F2 ] to 15sccm sink and the up electrode for O2, the high-frequency power of 800kHz and 1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into -20 degrees C. The etching rate of 610 nm/min and an interlayer oxide film 5 the etching rate of a nitride 4 Consequently, 570 nm/min, The dirty rate of etching rate 34 nm/min of a photoresist, a silicon substrate 1, and the capacity polysilicon plate 7 3 nm/min, The etching velocity ratio (selection ratio) of a nitride 4 and an interlayer oxide film 5 is abbreviation. 1.1 times, In the etching velocity ratio (selection ratio) of a nitride 4, a silicon substrate 1, and the capacity polysilicon plate 7, the etching velocity ratio (selection ratio) of about 200 times, an interlayer oxide film 5, a silicon substrate 1, and the capacity polysilicon plate 7 became about 190 times. Moreover, the etching configuration became a different direction-thing.
[0013] Here, the etching velocity ratio (selection ratio) to the interlayer oxide film of a nitride is abbreviation. With 1.1 times, although it is low, nitride etching has played not only nitride clearance but the role of additional etching (over etching) to just etching of the interlayer oxide film in the etching process of the above-mentioned interlayer oxide film.
[0014] According to the 1st operation gestalt of this invention, in the etching step of a nitride, etching of a nitride is promoted by C and H of CHxFy combining with N of a nitride, and generating C-N and N-H by adding the gas which contains hydrogen atoms, such as CHxFy gas, in fluorocarbon gas.
[0015] Moreover, since it uses the etching gas system almost equivalent to the etching gas system of the interlayer oxide film used for a nitride etching step in a contact etching step while the selectivity of CHxFy gas over silicon improves, since the deposition effectiveness is high gas, etching of it stabilized without changing the ambient atmosphere of an etching chamber is attained.
[0016] Next, the 2nd operation gestalt of this invention is explained using drawing 2 (a) - (c). This operation gestalt is what showed as an example contact etching in case the aspect ratio of contact is SRAM which is not so large, and drawing 2 is the sectional view showing the manufacture approach of the semiconductor device before and behind a contact etching chip in order of a process.
[0017] As shown in drawing 2 (a), the wrap interlayer oxide film 35 is formed [ electrode / the polish recon gate 32 and the tungsten silicide (WSi) 33 which constitute a gate electrode, the sidewall 36 which protects those side faces, and / a silicon substrate 31 and a gate electrode ] in the wrap nitride 34 and a nitride 34 on a silicon substrate 31, by photolithography technique, the pattern which has contact 41 is imprinted to a photoresist, and a photoresist 38 is formed.
[0018] Next, as shown in drawing 2 (b), dry etching of the etching (just etching) to a part for the thickness of an interlayer oxide film 35 is carried out with C4F8 / Ar/O2 mixed-gas plasma 39 by using a photoresist 38 as a mask using a 2 cycle RIE (Reactive IonEtching)

dry etching system. the conditions at this time -- 600sccm(s) were impressed for 7sccm(s) and Ar, the high-frequency power of 27MHz and 2000W was impressed [ $C_4F_8$ ] to 2sccm sink and the up electrode for $O_2$, the high-frequency power of 800kHz and 800W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 24mm, and substrate temperature was made into +20 degrees C in the bottom with a pressure of 6.67Pa. Consequently, in the etching velocity ratio (selection ratio) of 28 nm/min, an interlayer oxide film 35, and a photoresist 38, the etching velocity ratio (selection ratio) of about 15 times, an interlayer oxide film 35, and a nitride 34 became [ the etching rate of an interlayer oxide film 35 / the etching rate of 420 nm/min and a photoresist ] about 20 times.

[0019] Here, in etching of an interlayer oxide film, the aspect ratio of contact does not need to add CO to mixed gas highly [ the 1st operation gestalt ].

[0020] Then, as shown in drawing 2 (c), dry etching of the nitride 34 is carried out with $C_4F_8/CH_2F_2/Ar/O_2$ mixed gas 40. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 20sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ $C_4F_8$ / 10sccm(s) and $CH_2F_2$ ] to 15sccm sink and the up electrode for $O_2$, the high-frequency power of 800kHz and 1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into +20 degrees C. Consequently, for the dirty rate of 570 nm/min, etching rate 34 nm/min of a photoresist, and a silicon substrate 31, the etching velocity ratio (selection ratio) of 3 nm/min, a nitride 34, and an interlayer oxide film 35 is [ the etching rate of a nitride 34 / the etching rate of 610 nm/min and an interlayer oxide film 35 ] abbreviation. In the etching velocity ratio (selection ratio) of 1.1 times, a nitride 34, and a silicon substrate 31, the etching velocity ratio (selection ratio) of about 200 times, an interlayer oxide film 35, and a silicon substrate 31 became about 190 times. Moreover, the etching configuration became a different direction-thing.

[0021] Also in this operation gestalt, improvement in the etch selectivity to acceleration of nitride etching in the etching step of a nitride and silicon and good etching ** of productivity become possible like the 1st operation gestalt.

[0022] In addition, although $C_4F_8$ gas was used for the main reaction gas of nitride etching in the 1st of this invention, and the operation gestalt of 2, the same effectiveness is acquired even if it uses for reactant gas at least one kind chosen from the herd which consists of fluorocarbon gas, such as $C_3F_6$, $C_4F_6$, and $C_5F_8$ gas.

[0023] In the 1st of this invention, and the operation gestalt of 2 moreover, in the addition gas of nitride etching Although $CH_2F_2$ gas was used, monofluoromethane ($CH_3F$), a methyl bromide ($CH_3Br$), The same effectiveness is acquired, even if it uses for addition gas at least one kind chosen from the herd which consists of gas containing hydrogen atoms, such as $C_xH_yOH$ ($C_2H_5OH$, $CH_3OH$), or uses a carbon monoxide (CO) and a carbon dioxide ($CO_2$) for addition gas.

[0024] Furthermore, although $C_4F_8$ were used for the main reaction gas of interlayer oxide film etching in the 1st of this invention, and the operation gestalt of 2 The same effectiveness is acquired even if it uses for reactant gas at least one kind chosen from the herd which consists of fluorocarbon gas, such as $C_3F_6$, $C_4F_6$, and $C_5F_8$ gas, according to the main reaction gas of nitride etching. The same effectiveness is acquired even if it uses a carbon dioxide ($CO_2$) as addition gas in the 1st operation gestalt of this invention in addition to a carbon monoxide (CO).

[0025] Finally, in the 1st of this invention, and the operation gestalt of 2, the configuration

of each above-mentioned operation gestalt is mere instantiation at the etching step of a nitride, and the manufacture approach of the semiconductor device of this invention of including the manufacture approach of a semiconductor device of having added various corrections and modification which consist of the above-mentioned configuration is natural.

[0026]

[Effect of the Invention] As mentioned above, it sets to etching of the interlayer insulation film which consists of a laminated structure of a nitride and an oxide film. While etching of a nitride is promoted by using C4F8/CO/Ar/O2 mixed gas for etching of an oxide film, and using C4F8/CH2F2/Ar/O2 mixed gas for etching of the continuing nitride Since the deposition effectiveness is high gas, the selectivity of CHxFy gas over a silicone film improves. Furthermore, since the etching gas system almost equivalent to the etching gas system of the interlayer oxide film used for a nitride etching step in a contact etching step is used, good etching of productivity stabilized without changing the ambient atmosphere of an etching chamber is attained.

## TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the formation approach of the contact for taking connection to the component of a configuration of that the nitride and the oxide film were formed on the silicone film about the manufacture approach of a semiconductor device.

## PRIOR ART

[Description of the Prior Art] In recent years, in the field of a semiconductor device, it goes on increasingly, for example, the detailed-ization progresses about a VLSI, and reservation of the eye doubling margin of the photolithography technique in a contact formation process is becoming difficult. Then, the self aryne contact (SAC) technique of the contact etching technique which used the bonnet nitride as the stopper film for the gate electrode by the nitride in the contact formation process has become as [ use / technique / widely ].

[0003]

## EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, it sets to etching of the interlayer insulation film which consists of a laminated structure of a nitride and an oxide film. While etching of a nitride is promoted by using C4F8/CO/Ar/O2 mixed gas for etching of an oxide film, and using C4F8/CH2F2/Ar/O2 mixed gas for etching of the continuing nitride Since the deposition effectiveness is high gas, the selectivity of CHxFy gas over a silicone film improves. Furthermore, since the etching gas system almost equivalent to the etching gas

system of the interlayer oxide film used for a nitride etching step in a contact etching step is used, good etching of productivity stabilized without changing the ambient atmosphere of an etching chamber is attained.

## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, since interlayer insulation films, such as an oxide film, have covered the gate electrode a bonnet and on it by the nitride which is an insulator layer, in order to take connection with a gate electrode, it is necessary to form contact in an interlayer insulation film by contact etching, and to remove a nitride further in a self aryne contact process. In order to raise the omission nature in a nitride etching step, the oxygen flow rate needed to be made to increase as the aspect ratio of contact becomes high although CHF3/O2-/Ar mixed gas etc. has been conventionally used for nitride clearance after this contact etching. Therefore, the instability of the process by change of the chamber ambient atmosphere by the difference between frequent occurrence of the dust by peeling of the deposition which the selectivity of the capacity polysilicon plate and the silicon substrate which have been exposed at the time of nitride etching, and a nitride fell, could delete the thrust omission of capacity polysilicon and the silicon substrate, and did not come to accept, but was deposited on the breadth of the diameter of contact by lowering of selectivity with a resist and an etching chamber side attachment wall, and the etching gas system of a contact etching step and a nitride etching step was a problem.
[0004] The object of this invention is in the dry etching of the interlayer film which consists of a laminated structure of a nitride and an oxide film to offer the manufacture approach of the semiconductor device whose high productivity becomes possible, without being able to carry out improvement in a selection ratio with a resist and silicon, and controlling generating of dust, and changing a chamber ambient atmosphere.

## MEANS

[Means for Solving the Problem] As for the manufacture approach of the semiconductor device of this invention, a lower layer forms [ a nitride and the upper layer ] the cascade screen which consists of an oxide film above a substrate. Carry out etching clearance of said oxide film selectively using the 1st etching gas, and opening is formed in said oxide film. It is the manufacture approach of the semiconductor device which carries out etching clearance of said nitride through said opening using the 2nd etching gas. Said 2nd etching gas It is characterized by consisting of mixed gas which made CxFy main reaction gas. CxFy of said 2nd etching gas It is gas of C3F6, C4F6, C4F8, or C5F8. Said 2nd etching gas CH2F2, CH3F, and CH3 -- the gas of the Br, NH3, C2H5OH, or the CH3OH(s) is included by said 2nd etching gas as addition gas, or the gas of either CO or COs2 is included as addition gas
[0006] Moreover, in the manufacture approach of the above-mentioned semiconductor

device, said 1st etching gas is mixed gas which makes the same CxFy as the main reaction gas of said 2nd etching gas main reaction gas, and, in said 1st etching gas, said both 1st etching gas and said 2nd etching gas contain Ar and O2 including the gas of either CO or CO2 as addition gas.
[0007] In the manufacture approach of the above-mentioned semiconductor device, the etching process by said 2nd etching gas is continuously performed at the last within the same chamber as said 1st etching following the etching process by said 1st etching gas.
[0008]
[Embodiment of the Invention] First, the 1st operation gestalt of this invention is explained using drawing 1 (a) - (c). This operation gestalt is DRAM which makes the tantalum oxide film etc. capacity, it is what showed contact etching when the aspect ratio of contact is large as an example, and drawing 1 is the sectional view showing the manufacture approach of the semiconductor device before and behind a contact etching chip in order of a process.
[0009] As shown in drawing 1 (a), the wrap nitride 4, the tantalum oxide (Ta 2O5) 6 which constitutes the capacity in which a silicon substrate 1 and a nitride 4 are further formed into the wrap interlayer oxide film 5 and an interlayer oxide film 5, and the capacity polysilicon plate 7 are formed on a silicon substrate 1 in the polish recon gate 2, the tungsten silicide (WSi) 3, and it which constitute a gate electrode, by photolithography technique, the pattern which has contact 11 is imprinted to a photoresist, and a photoresist 8 is formed.
[0010] Next, as shown in drawing 1 (b), dry etching of the etching (just etching) to a part for the thickest thickness of an interlayer oxide film 5 is carried out with C4F8 / CO/Ar/O2 mixed gas 9 by using a photoresist 8 as a mask using a 2 cycle RIE (Reactive IonEtching) dry etching system. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 40sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ C4F8 / 20sccm(s) and CO ] to 9sccm sink and the up electrode for O2, the high-frequency power of 800kHz and 1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into -20 degrees C. Consequently, in the etching rate of 730 nm/min and a photoresist, the etching velocity ratio (selection ratio) of 79 nm/min, an interlayer oxide film 5, and a photoresist 8 is [ the etching rate of an interlayer oxide film 5 ] about 9 times.
[0011] In etching of the above-mentioned interlayer oxide film, in order to make etching gas permeate contact of a high aspect ratio, it is effective in mixed gas to add CO.
[0012] Then, as shown in drawing 1 (c), dry etching of the nitride 4 is carried out with C4F8/CH2F2/Ar/O2 mixed gas 10. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 20sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ C4F8 / 10sccm(s) and CH2F2 ] to 15sccm sink and the up electrode for O2, the high-frequency power of 800kHz and 1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into -20 degrees C. The etching rate of 610 nm/min and an interlayer oxide film 5 the etching rate of a nitride 4 Consequently, 570 nm/min, The dirty rate of etching rate 34 nm/min of a photoresist, a silicon substrate 1, and the capacity polysilicon plate 7 3 nm/min, The etching velocity ratio (selection ratio) of a nitride 4 and an interlayer oxide film 5 is abbreviation. 1.1 times, In the etching velocity ratio (selection ratio) of a nitride 4, a silicon substrate 1, and the

capacity polysilicon plate 7, the etching velocity ratio (selection ratio) of about 200 times, an interlayer oxide film 5, a silicon substrate 1, and the capacity polysilicon plate 7 became about 190 times. Moreover, the etching configuration became a different direction-thing.

[0013] Here, the etching velocity ratio (selection ratio) to the interlayer oxide film of a nitride is abbreviation. With 1.1 times, although it is low, nitride etching has played not only nitride clearance but the role of additional etching (over etching) to just etching of the interlayer oxide film in the etching process of the above-mentioned interlayer oxide film.

[0014] According to the 1st operation gestalt of this invention, in the etching step of a nitride, etching of a nitride is promoted by C and H of CHxFy combining with N of a nitride, and generating C-N and N-H by adding the gas which contains hydrogen atoms, such as CHxFy gas, in fluorocarbon gas.

[0015] Moreover, since it uses the etching gas system almost equivalent to the etching gas system of the interlayer oxide film used for a nitride etching step in a contact etching step while the selectivity of CHxFy gas over silicon improves, since the deposition effectiveness is high gas, etching of it stabilized without changing the ambient atmosphere of an etching chamber is attained.

[0016] Next, the 2nd operation gestalt of this invention is explained using drawing 2 (a) - (c). This operation gestalt is what showed as an example contact etching in case the aspect ratio of contact is SRAM which is not so large, and drawing 2 is the sectional view showing the manufacture approach of the semiconductor device before and behind a contact etching chip in order of a process.

[0017] As shown in drawing 2 (a), the wrap interlayer oxide film 35 is formed [ electrode / the polish recon gate 32 and the tungsten silicide (WSi) 33 which constitute a gate electrode, the sidewall 36 which protects those side faces, and / a silicon substrate 31 and a gate electrode ] in the wrap nitride 34 and a nitride 34 on a silicon substrate 31, by photolithography technique, the pattern which has contact 41 is imprinted to a photoresist, and a photoresist 38 is formed.

[0018] Next, as shown in drawing 2 (b), dry etching of the etching (just etching) to a part for the thickness of an interlayer oxide film 35 is carried out with C4F8 / Ar/O2 mixed-gas plasma 39 by using a photoresist 38 as a mask using a 2 cycle RIE (Reactive IonEtching) dry etching system. the conditions at this time -- 600sccm(s) were impressed for 7sccm(s) and Ar, the high-frequency power of 27MHz and 2000W was impressed [ C4F8 ] to 2sccm sink and the up electrode for O2, the high-frequency power of 800kHz and 800W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 24mm, and substrate temperature was made into +20 degrees C in the bottom with a pressure of 6.67Pa. Consequently, in the etching velocity ratio (selection ratio) of 28 nm/min, an interlayer oxide film 35, and a photoresist 38, the etching velocity ratio (selection ratio) of about 15 times, an interlayer oxide film 35, and a nitride 34 became [ the etching rate of an interlayer oxide film 35 / the etching rate of 420 nm/min and a photoresist ] about 20 times.

[0019] Here, in etching of an interlayer oxide film, the aspect ratio of contact does not need to add CO to mixed gas highly [ the 1st operation gestalt ].

[0020] Then, as shown in drawing 2 (c), dry etching of the nitride 34 is carried out with C4F8/CH2F2/Ar/O2 mixed gas 40. the conditions at this time -- the bottom with a pressure of 5.33Pa -- 500sccm(s) were impressed for 20sccm(s) and Ar, the high-frequency power of 27MHz and 2200W was impressed [ C4F8 / 10sccm(s) and CH2F2 ] to 15sccm sink and the up electrode for O2, the high-frequency power of 800kHz and

1400W was impressed to the substrate, spacing of an up electrode and a lower electrode was set as 20mm, and substrate temperature was made into +20 degrees C. Consequently, for the dirty rate of 570 nm/min, etching rate 34 nm/min of a photoresist, and a silicon substrate 31, the etching velocity ratio (selection ratio) of 3 nm/min, a nitride 34, and an interlayer oxide film 35 is [ the etching rate of a nitride 34 / the etching rate of 610 nm/min and an interlayer oxide film 35 ] abbreviation. In the etching velocity ratio (selection ratio) of 1.1 times, a nitride 34, and a silicon substrate 31, the etching velocity ratio (selection ratio) of about 200 times, an interlayer oxide film 35, and a silicon substrate 31 became about 190 times. Moreover, the etching configuration became a different direction-thing.
[0021] Also in this operation gestalt, improvement in the etch selectivity to acceleration of nitride etching in the etching step of a nitride and silicon and good etching ** of productivity become possible like the 1st operation gestalt.
[0022] In addition, although C4F8 gas was used for the main reaction gas of nitride etching in the 1st of this invention, and the operation gestalt of 2, the same effectiveness is acquired even if it uses for reactant gas at least one kind chosen from the herd which consists of fluorocarbon gas, such as C3F6, C4F6, and C5F8 gas.
[0023] In the 1st of this invention, and the operation gestalt of 2 moreover, in the addition gas of nitride etching Although CH2F2 gas was used, monofluoromethane (CH3F), a methyl bromide (CH3Br), The same effectiveness is acquired, even if it uses for addition gas at least one kind chosen from the herd which consists of gas containing hydrogen atoms, such as CxHyOH (C2H5OH, CH3OH), or uses a carbon monoxide (CO) and a carbon dioxide (CO2) for addition gas.
[0024] Furthermore, although C4F8 were used for the main reaction gas of interlayer oxide film etching in the 1st of this invention, and the operation gestalt of 2 The same effectiveness is acquired even if it uses for reactant gas at least one kind chosen from the herd which consists of fluorocarbon gas, such as C3F6, C4F6, and C5F8 gas, according to the main reaction gas of nitride etching. The same effectiveness is acquired even if it uses a carbon dioxide (CO2) as addition gas in the 1st operation gestalt of this invention in addition to a carbon monoxide (CO).
[0025] Finally, in the 1st of this invention, and the operation gestalt of 2, the configuration of each above-mentioned operation gestalt is mere instantiation at the etching step of a nitride, and the manufacture approach of the semiconductor device of this invention of including the manufacture approach of a semiconductor device of having added various corrections and modification which consist of the above-mentioned configuration is natural.

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the manufacture approach of the semiconductor device of the 1st operation gestalt of this invention in order of a process.
[Drawing 2] It is the sectional view showing the manufacture approach of the semiconductor device of the 2nd operation gestalt of this invention in order of a process.
[Description of Notations]
1 31 Silicon semi-conductor substrate
2 32 Polish recon gate
3 33 WSi

4 34 Nitride
5 35 Interlayer oxide film
6 Tantalum Oxide
7 Capacity Polysilicon Plate
8 38 Photoresist
9, 10, 39, 40 Mixed gas
11 41 Contact
36 Sidewall

CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of the semiconductor device characterized by to be the manufacture approach of the semiconductor device which a lower layer forms a nitride and the cascade screen which the upper layer becomes from an oxide film, and carries out etching clearance of said oxide film selectively using the 1st etching gas, forms opening above a substrate at said oxide film, and carries out etching clearance of said nitride through said opening using the 2nd etching gas, and for said 2nd etching gas to consist of mixed gas which made CxFy main reaction gas.
[Claim 2] CxFy of said 2nd etching gas is the manufacture approach of the semiconductor device according to claim 1 which is gas of C3F6, C4F6, C4F8, or C5F8.
[Claim 3] said 2nd etching gas -- CH2F2, CH3F, and CH3 -- the manufacture approach of the semiconductor device according to claim 2 which contains the gas of the Br, NH3, C2H5OH, or the CH3OH(s) as addition gas.
[Claim 4] Said 2nd etching gas is the manufacture approach of the semiconductor device according to claim 2 which contains the gas of either CO or COs2 as addition gas.
[Claim 5] Said 1st etching gas is the manufacture approach of the semiconductor device according to claim 2, 3, or 4 which is the mixed gas which makes the same CxFy as the main reaction gas of said 2nd etching gas main reaction gas.
[Claim 6] Said 1st etching gas is the manufacture approach of the semiconductor device according to claim 5 which contains the gas of either CO or CO2 as addition gas.
[Claim 7] Said both 1st etching gas and said 2nd etching gas are the manufacture approach of the semiconductor device containing Ar and O2 according to claim 1, 2, 3, 4, 5, or 6.
[Claim 8] The etching process by said 2nd etching gas is the manufacture approach of the semiconductor device according to claim 1, 2, 3, 4, 5, 6, or 7 continuously performed within the same chamber as said 1st etching following the etching process by said 1st etching gas.

[Translation done.]

[Translation done.]